

# A 0.0025mm<sup>2</sup> Bandgap Voltage Reference for 1.1Volt supply in Standard 0.16μm CMOS

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## **Abstract:**

A sub-1V bandgap voltage reference (BGVR) in 0.16μm CMOS is presented that circumvents the trade-off between area and power consumption in conventional sub-1V BGVR topologies. This circuit can be used in systems to generate reference voltages locally, eliminating the conventional relatively large BGVR and its global reference voltage distribution interconnect. The active area is 0.0025mm<sup>2</sup>; at 295K,  $V_{REF}=0.94V$  with  $\sigma=0.8\%$  at a minimum supply voltage of 1.1V, with 1.4μA supply current.

## **Text:**

Today's ICs usually employ one bandgap voltage reference (BGVR) circuit to generate a well defined voltage that is reused at many places in that IC. The classical BGVR generates a reference voltage that is slightly larger than the material bandgap: a little above 1200mV in silicon. For deep sub-micron technologies the supply voltage is about the same as the material bandgap which prevents using the classical bandgap structure. As a solution a number of BGVR topologies that create a sub-1V are invented; most of them are based on the structure introduced by Banba [1], some are using resistive voltage division [2] or voltage averaging [3]. For low-

power operation high-ohmic resistors (occupying a large area!) must be used in all these techniques, leading to an immediate trade-off between power consumption and chip-area. This trade-off prevents the local generation of reference voltages where they are required: either the power penalty or the area penalty would be too significant. Alternative topologies that do not require high-ohmic resistors typically are not-BGVR-based circuits relying on threshold voltages and hence require trimming to achieve low spread.

The current manuscript presents a sub-1V BGVR that circumvents the power-area trade off of conventional sub-1V BGVR, aiming at local reference voltage generation wherever a reference voltage is needed in a die. To break the power-area trade-off no resistive averaging nor subdivision can be used to get sub-1V operation, while a drive to minimum area results in avoiding any topology using opamps, high ohmic resistors or multiple diodes. The basic topology of the BGVR is shown in Fig. 1 and is known [4]. For this topology and assuming that the PMOS transistors  $MP_1$  and  $MP_2$  are in weak-inversion with an ideal exponential behavior, the generated reference voltage ( $V_{REF}$ ) is known to be  $V_{REF} = \frac{kT}{q} \cdot N \cdot \ln(A) + \frac{kT}{q} \cdot \ln\left(\frac{I_C(T)}{I_{C,0} \cdot T^\eta}\right) + V_{gap,0} \approx 1.2V$ , with a curvature that amounts to about 4mV over a 160K temperature range. In this relation the factor  $N$  equals the ratio between resistors  $R_2$  and  $R_1$ , the factor  $A$  equals the ratio of the current factors of transistors  $MP_1$  and  $MP_2$ ,  $I_C(T)$  is the diode current as a function of temperature  $T$ ,  $\eta$  is a technology and topology dependent factor typically around 4 while the other parameters are technology dependent or just plain constants. For actual, non-ideal, weak-inversion operated MOS transistors the expression for  $V_{REF}$  is more complex, which is not of main relevance for the current manuscript.

To get a sub-1V BGVR without any subdivision, we introduce an almost temperature independent offset between  $MP_1$  and  $MP_2$ , realized using the dependency between threshold

voltage  $V_T$  and transistor length  $L$ . A typical  $V_T(L)$  relation for three temperatures is given in Fig. 2. On the x-axis in this figure is the transistor length, starting at minimum length. With increasing length the  $V_T$  first increases and then decreases, due to short channel effects [5]. For the current circuit we selected transistor lengths  $L_1$  and  $L_2$  for transistors  $MP_1$  and  $MP_2$  respectively, yielding an almost temperature independent offset voltage  $\Delta V_T$ . The results is that now

$$V_{REF} = N \cdot \left[ \frac{kT}{q} \cdot \ln(A) - \Delta V_T \right] + \frac{kT}{q} \cdot \ln \left( \frac{I_C(T)}{I_{C,0} \cdot T^\eta} \right) + V_{gap,0} \approx 1.2V - N \cdot \Delta V_T. \quad (1)$$

An associated effect is that the BGVR does not operate at temperatures below  $T_{min} = \frac{q \cdot \Delta V_T}{k \cdot \ln(A)}$ , whereas a conventional BGVR has a lower temperature limit that is set by some other limitations of the circuitry in the BGVR or is determined just by the application; a typical lower useful temperature limit is  $-25^\circ\text{C}$  or  $-40^\circ\text{C}$ ; reaching  $-273^\circ\text{C}$  (0 K) is not often necessary. To put it the other way round, if the BGVR of Fig. 1 must operate down to a temperature  $T_{min}$ , the minimum  $V_{REF} \approx 1.2V - (T_{min} - 273.15) \cdot \frac{2mV}{K}$ . The 2mV/K in this relation corresponds to the temperature dependency of a PN-junction at constant or weakly temperature dependent current.

The circuit we implemented equals the principle circuit of Fig. 1, with regulated cascodes, see Fig. 3. For the design, a minimum usable temperature of  $-40^\circ\text{C}$  was defined, with a design margin of  $60^\circ\text{C}$ , which yields effectively  $T_{min} = -100^\circ\text{C}$  and results in  $V_{REF} \approx 900mV$ . In our design we did some extra optimization in the length ratios and width ratios of the transistors to get maximum curvature correction. The designed circuit measures  $50\mu\text{m} * 50\mu\text{m}$  in standard  $0.16\mu\text{m}$  bulk CMOS technology. Measurements were done on a Süss Microtec PM200 wafer prober with cooling, using a Keithley 4200 analyzer.

Fig. 4 shows the generated  $V_{REF}$  and supply current  $I_{DD}$  as a function of the supply voltage  $V_{DD}$ , for  $-45^{\circ}\text{C}$ ,  $25^{\circ}\text{C}$  and  $145^{\circ}\text{C}$  for one sample. Note that the  $V_{REF}$  curves are almost overlapping; only the curve for  $145^{\circ}\text{C}$  shows a slight deviation from the others. As expected, the  $I_{DD}$  curves are very much different, approximately corresponding to an offset proportional-to-temperature current. Fig. 5 shows  $V_{REF}$  and  $I_{DD}$  as a function of temperature for one sample (with a near average  $V_{REF}$ ) at  $V_{DD}=1.2\text{V}$ ; note that the  $V_{REF}$ -axis is zoomed in to be able to visualize any variation in the reference voltage. Also visible in the figure is the small curvature in the  $I_{DD}$ -curve which was designed for maximum curvature correction. Extrapolation of this non-linear curve shows a  $T_{min} \approx -120^{\circ}\text{C}$  which nicely complies with the measured  $V_{REF} \approx 940\text{mV}$ . As for any BGVR, sufficiently low spread is essential; the upper part of Fig. 5 shows the measured  $V_{REF}$  for 60 (untrimmed and unselected) samples at  $V_{DD}=1.2\text{V}$  and at  $23^{\circ}\text{C}$ ; the sample used for the lower part in Fig. 5 is sample 33. From this the average  $V_{REF}$  equals  $944\text{mV}$  with a 1 sigma spread figure  $\sigma_{V_{REF}}=0.76\%$ . A micrograph of the chip is shown in Fig. 7, in which the sub-1V BGVR is inside the black square.

The comparison chart in Fig. 6 shows properties of a number of published sub-1V CMOS voltage reference circuits that include measured spread data. Standard bandgap voltage references producing the conventional 1.2V and BiCMOS circuits were not taken into account. The data in Fig. 6 shows that the presented sub-1V BGVR has good untrimmed performance (reference voltage spread  $\sigma_{V_{REF}}$  and temperature coefficient  $TC$ ) at simultaneously a low power consumption and a low area consumption.

In summary, an ultra-compact sub-1V BGVR that circumvents the usual power-area trade off is presented, operating at  $1.4\mu\text{A}$  at room temperature with supply voltages down to  $1.1\text{V}$ ,

generating  $V_{REF}=0.94V$  with  $\sigma=0.76\%$ , with an active area of  $50\mu m * 50\mu m$  in  $0.16\mu m$  CMOS technology. These specifications enable local generation of reference voltages wherever needed.

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**Figure captions:**

**Figure 1: Principle schematic of the area efficient low-power sub-1V BGVR circuit: a conventional CTAT voltage ( $V_D$ ) is added to a down-shifted PTAT voltage ( $V_{R2}$ ).**

**Figure 2: Typical threshold voltage ( $V_T$ ) dependency on transistor length in modern CMOS technologies for 3 temperatures: using a balanced pair using lengths  $L_1$  and  $L_2$  creates an almost constant offset voltage  $\Delta V_T$ .**

**Figure 3: Actual circuit implementation: the circuit of Fig. 2 with regulated cascades.**

**Figure 4: Measured output voltage  $V_{REF}$  and supply current  $I_{DD}$  of the BGVR as a function of supply voltage  $V_{DD}$ , at  $T = -45^\circ\text{C}$ ,  $T = 25^\circ\text{C}$  and  $T = 145^\circ\text{C}$ .**

**Figure 5: Upper: measured  $V_{REF}$  on 60 samples at a supply voltage  $V_{DD} = 1.2\text{V}$  at  $23^\circ\text{C}$ : average  $V_{REF} = 944\text{mV}$  with  $\sigma_{V_{REF}} = 0.8\%$ ; lower: measured  $V_{REF}$  and  $I_{DD}$  as a function of temperature at  $V_{DD} = 1.2\text{V}$  for a near average sample (sample 33 in upper part)**

**Figure 6: Comparison of reported sub-1V voltage references in CMOS.**

**Figure 7: Micrograph of the chip fabricated in a standard 160nm bulk CMOS; the sub-1V bandgap voltage reference circuit is inside the black square.**

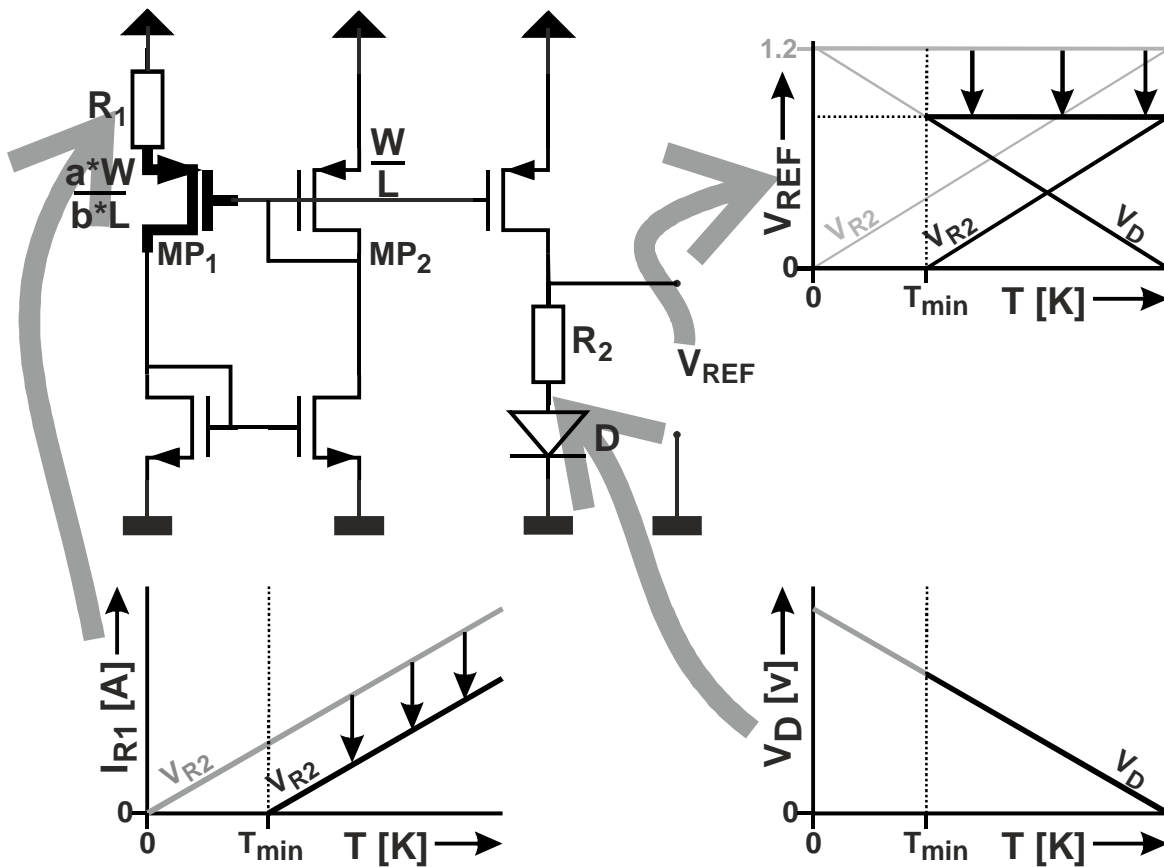
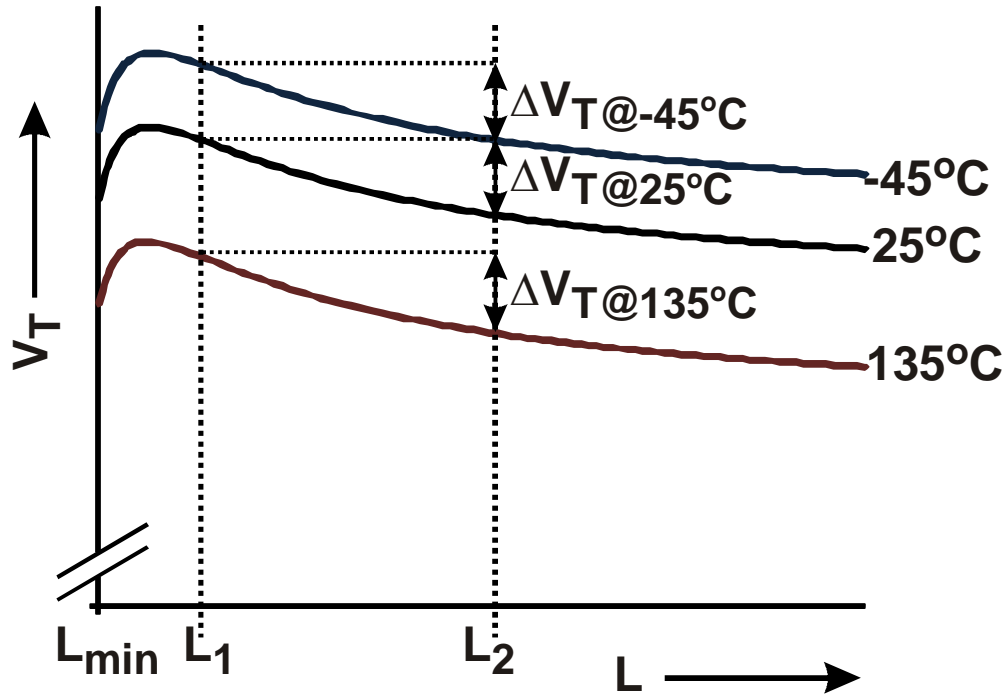


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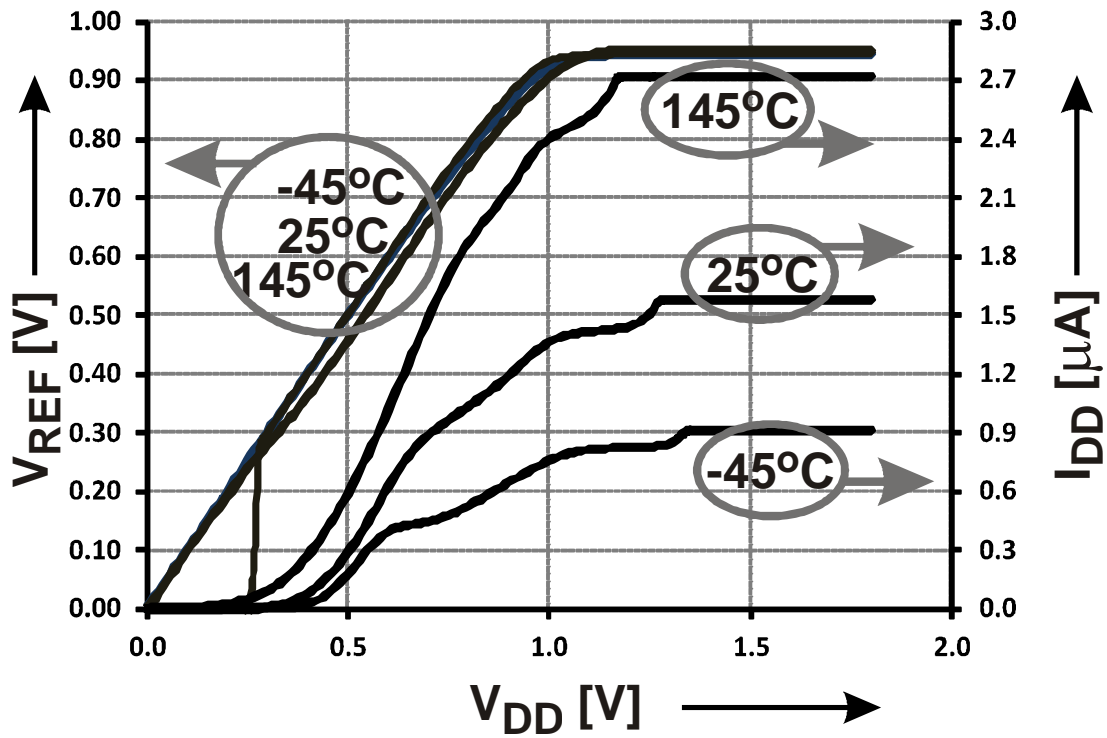
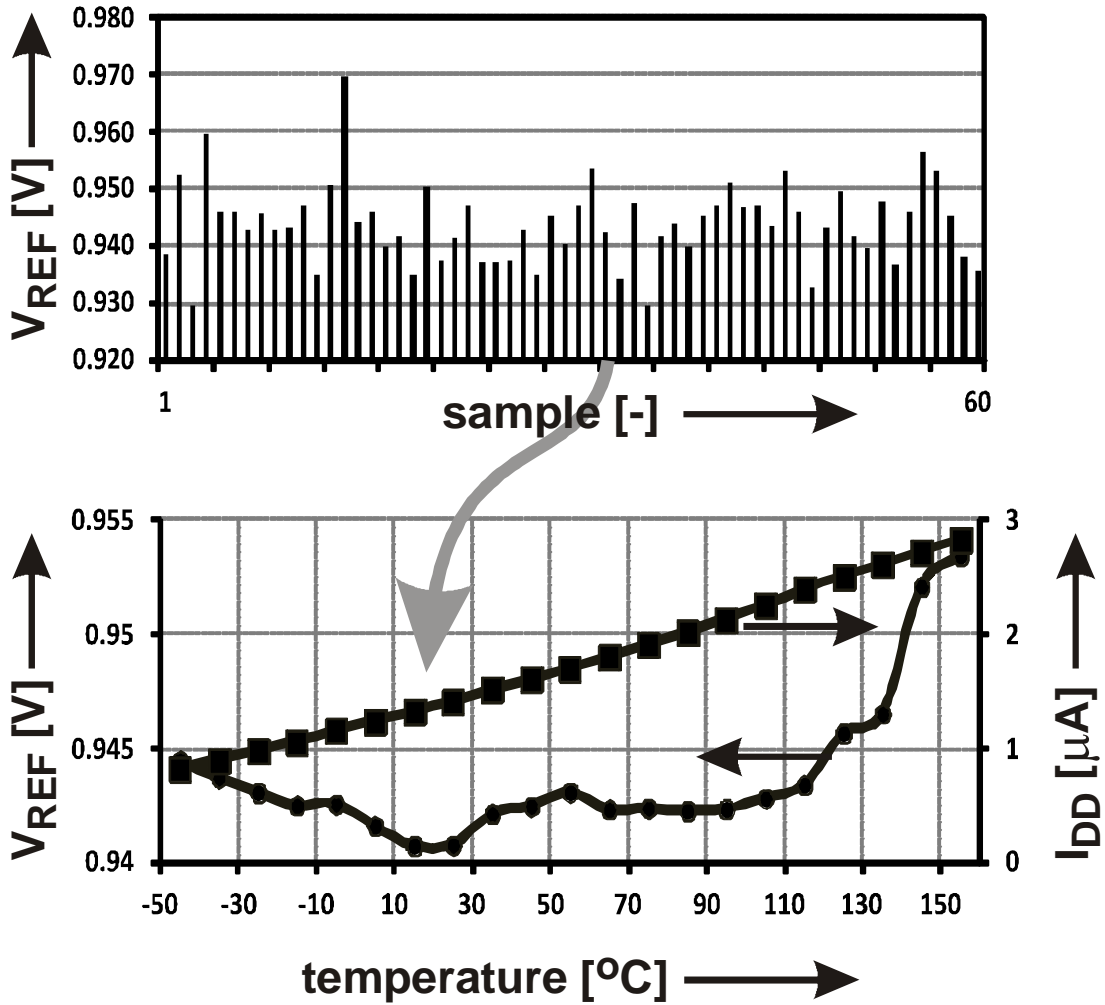


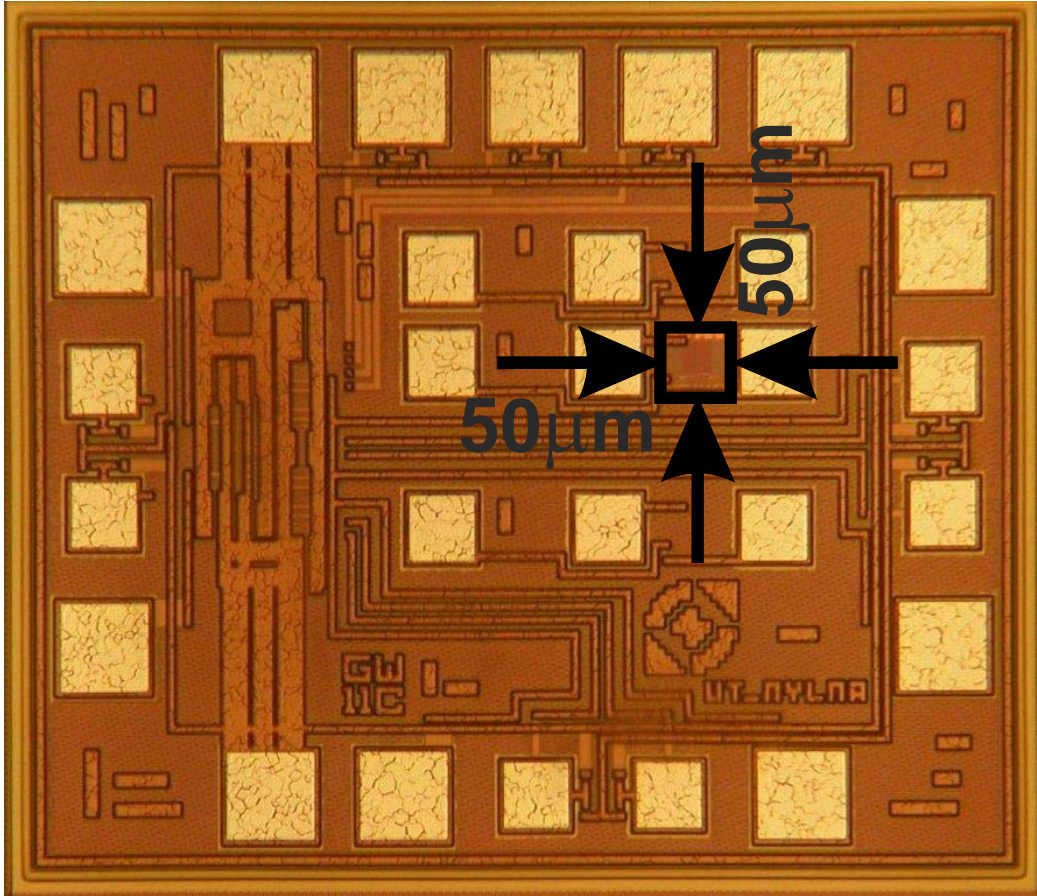
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	[2]	[6]	[7]	[8]	[9]	This work
<b>Technology (all CMOS)</b>	<b>0.35<math>\mu</math>m</b>	<b>0.35<math>\mu</math>m</b>	<b>0.5<math>\mu</math>m</b>	<b>0.6<math>\mu</math>m</b>	<b>0.35<math>\mu</math>m</b>	<b>0.16<math>\mu</math>m</b>
<b>V<sub>DD</sub></b>	<b>&gt;1.4V</b>	<b>&gt;1V</b>	<b>&gt;0.95V</b>	<b>&gt;0.98V</b>	<b>&gt;0.85V</b>	<b>&gt;1.1V</b>
<b>V<sub>REF</sub></b>	<b>858mV</b>	<b>190.1mV</b>	<b>628mV</b>	<b>603mV</b>	<b>650mV</b>	<b>944mV</b>
<b><math>\sigma_{VREF}</math></b>	<b>trimmed</b>	<b>~0.9%</b>	<b>0.26%</b>	<b>~0.5%</b>	<b>~1%</b>	
	<b>untrimmed</b>					<b>2%</b> <b>0.8%</b>
<b>min temp max temp</b>	<b>-20°C 120°C</b>	<b>-20°C 120°C</b>	<b>-40°C 120°C</b>	<b>0°C 100°C</b>	<b>-20°C 100°C</b>	<b>-45°C 135°C</b>
<b>TC</b>	<b>trimmed</b>	<b>12.4ppm/°C</b>	<b>16.9ppm/°C</b>	<b>17ppm/°C</b>	<b>&lt;25ppm/°C</b>	
	<b>untrimmed</b>			<b>670ppm/°C</b>		<b>60 ppm/°C</b> <b>30ppm/°C</b>
<b>I<sub>DD</sub>@~300K</b>	<b>116<math>\mu</math>A</b>	<b>0.25 <math>\mu</math>A - 0.56<math>\mu</math>A</b>	<b>&lt;10<math>\mu</math>A</b>	<b>&lt;18<math>\mu</math>A</b>	<b>1.2<math>\mu</math>A</b>	<b>1.4<math>\mu</math>A</b>
<b>Area</b>	<b>1.2mm<sup>2</sup></b>	<b>0.049 mm<sup>2</sup></b>	<b>1.1mm<sup>2</sup></b>	<b>0.24mm<sup>2</sup></b>	<b>0.063 mm<sup>2</sup></b>	<b>0.0025mm<sup>2</sup></b>

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