A Fully Integrated 8-channel Wide-Band Receiver for Ku-band Dual-Polarization Phased Array in SiGe BiCMOS

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***Abstract*— A Ku-band fully-integrated 8-channel phased-array receiver with 2GHz wide IF-bandwidth on a 3.8*4mm die is presented. The receiver has extensive processing at IF-level, like polarization discrimination, but it consumes only 132mW per channel. Each channel has 40dB gain and a IP1dB of -66dBm. The wide bandwidth calls for constant group-delay implementations in the IF chain. A novel bipolar implementation for true time delay is proposed, with a continuous programmable delay range of 0...100ps.**

An active, linear-phase, poly-phase IF-filter at 1…3GHz is used. The high level of integration makes it possible to build an ultra-flat (1cm) array antenna with high resolution beam-forming.

***Keywords*—Phased arrays, satellite receiver, true time delay, poly phase band-pass filter, dual polarization, wide bandwidth, ultra flat antenna, gyrators.**

I. INTRODUCTION

The subject of this paper is a Ku-band satellite-tracking receiver chip to realize an ultra-flat phased-array antenna for moving-vehicles [0]. Tracking calls for active elevation and azimuth (θ,ϕ) beam-steering, but also for active polarization discrimination. The application demands simultaneous reception of TV-signals in two separate satellite bands. This requires a bandwidth (BW) of 2GHz at ~12GHz RF. Within this BW, group-delay variations over frequency must be minimized to avoid dispersion of data signals.

Traditional phased-array solutions suffer from limited BW [1] and/or limited processing capabilities like polarization discrimination [1-2]. In this receiver these items are addressed by using full post-processing at IF-level. Because of the high BW, traditional phase-compensation for the antenna elements (AEs) cannot be used because this would make the beam-shape deform over frequency (beam-squint).

Therefore true time delays (TTD) are used, which must be placed in either the RF-path [2-3] or the IF-path [this work]. Some solutions have limited resolutions [1-3]. This work uses a continuous group-delay adjustment, resulting in a novel implementation for TTD. Processing at IF-level offers low power consumption because of the lower frequency (1…3GHz). TTD correction at IF-level avoids multiple LO-distribution paths as used in other solutions [1] as this would increase power-consumption. Further post-processing offers complete polarization discrimination, delivering true Vertical and Horizontal (V-H) outputs, while the antenna receives a random rotation angle (φ) of polarization. Direction parameters (θ,ϕ and φ) are fed to the chip real-time, in order to keep the beam focused at the satellite.

II. SYSTEM OVERVIEW

The system consists of two different types of RFICs, realized in NXP's QUBIC4-Xi BiCMOS SiGe 0.25um process technology. The first (RFIC1) handles a subset of four dual-polarization stacked patch AEs [4]. RFIC1 combines the output of 4 AEs (i.e. 8 RF input signals). Each input has its own front-end (Fig.1) providing low noise amplification, down conversion, IF filtering, mixer phase correction, and TTD. After summation of 4 channels, there is polarization discrimination and a variable gain (VGA) output driver.

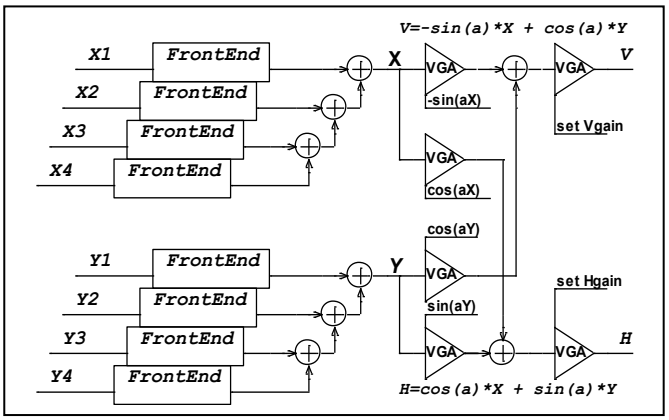

Fig.1. RFIC1: eight X/Y frontend-channels combined to 1 V/H output

The outputs are two differential IF signals, one for each polarization (V and H). The outputs of four RFIC1s are combined by the second chip, RFIC2. RFIC2 provides an input buffer, longer TTD, summation of 4 RFIC1 outputs, and a variable gain output buffer. RFIC2 will not be discussed in this paper.

The receiver channels are designed with fully symmetrical signal paths to minimize substrate coupling and EMI to adjacent channels. For the same reason, the channels are placed some physical distance (~200μm) apart. The channels must be as identical as possible to present the same phase delay and gain. Small differences are calibrated out with the adjustable TTDs and VGAs. All IC-cells are designed with voltage in/outputs to avoid power loss in termination resistors. Summation is done with currents. Two I/Q generators/drivers are included for the LO distribution using micro-strip because

of the longer distribution-length. Each generator drives 4 channels and has a considerable power consumption of 135mW, due to the need for termination resistors at the micro-strips. Two drivers per side are used for easy routing over the chip, so LO-distribution is limited to eight micro-strips per side. A master-LO signal of 9.75GHz is provided externally.

III. RECEIVER CHANNEL RFIC1

The receiver front-end is set up as a low-IF system. Quadrature down-mixing is used in combination with a band-pass filter (BPF) to suppress images. The LNA features a tank circuit to provide additional suppression of the image band.

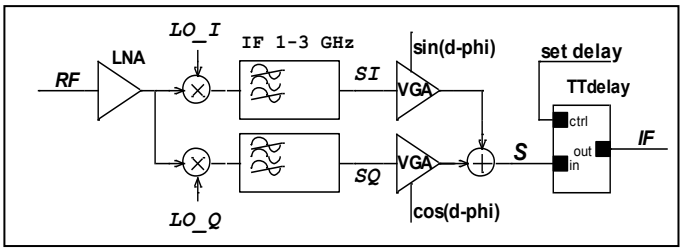

Fig.2. Front-end channel in RFIC1

A constant group-delay within the whole IF-chain over the full BW is crucial. The IF-range from 1…3GHz is carefully chosen to prevent spurious and harmonic products to fall in the IF-band. The frequency is low enough for power-efficient IF-processing. A continuous-time active poly-phase (APP) BPF was designed to create 2GHz of IF-bandwidth with minimal group-delay variations. TTDs are used at IF for the same reason. The shift in frequency from RF to IF has consequences for the delay requirements [5]. For beam-forming at IF, it is required that the initial time difference τ between antenna signals also appears at IF.

It can be shown that after mixing also a phase shift occurs which depends on τ and the LO frequency (ωo) [5]:

$$\Delta\varphi = -\omega o \cdot \tau + (\varphi 1 - \varphi 2) \quad (1)$$

where $\varphi 1$ and $\varphi 2$ are the initial phases of the two RF signals. The SI/SQ signals at the BPF outputs (see Fig.2) are used to construct a vector modulator to correct this according to:

$$S = SI \cdot \sin(\Delta\varphi) + SQ \cdot \cos(\Delta\varphi) \quad (2)$$

To suppress the noise of all post-processing, the LNA has 22dB gain and the mixer has a conversion gain of 12dB.

IV. ACTIVE POLY PHASE BANDPASS FILTER

The I/Q signals from the mixers can be utilized to add complex poles to a set of second order low-pass filters (LPFs) to achieve an active BPF [6].

Two cross-coupled gyrators Gc (Fig. 3) transform the low-pass function into a band-pass function by shifting ω_n of the LPF to a higher positive frequency [7]. This way IF filtering can be made active and tunable by manipulating the gyration constants with little group-delay variation. The LPFs are implemented as fully differential, second order bi-quads. When ω_{IF} is the desired center frequency of the BPF, the gm of the cross-gyrators is given by:

$$Gc = \omega_{IF} \cdot C \quad (4)$$

The bandwidth is given by:

$$BW = 2 \cdot \omega_n = 2 \cdot Gm/C \quad (5)$$

The simulated total-channel image rejection is 20dB.

Since the IF-filter operates from 1 to 3 GHz, the current-conveyors in the gyrators must have at least 3 times more bandwidth to not disturb the filter performance. This calls for a non-complex implementation setup.

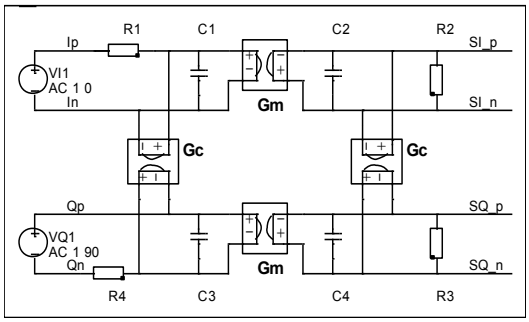

Fig.3. Differential second order active poly-phase BPF

The gyrators are implemented with simple differential pairs with current-mode feedback (Fig.4). Bias-current was chosen as low as 400uA per transistor for an Ft of 43GHz of the HBTs. An emitter resistance Rgm provides the feedback, extending the conveyor bandwidth to over 10 GHz. Rgm also linearizes the large-signal transfer, improving IP3 and 1dB compression point. The gyrator constant is approximated with:

$$gm = 1/((2.k.T)/(q.Ie) + Rgm) \quad (6)$$

Rgm is chosen only ~4 times higher than kT/(q.Ie), so that the transfer gm can still be manipulated with the transistors bias-current Ie. Since temperature is part of the expression, gm is stabilized with a PTAT bias current. It is important to keep common-mode (CM) gain below unity in all sub-cells to prevent CM oscillations.

Therefore a CM-feedback circuit is used, which also fixes the voltages at the collectors of Q1…Q4. The PMOS current sources M1…M4 have a feedback for CM only via M5/6 and R1…R4.

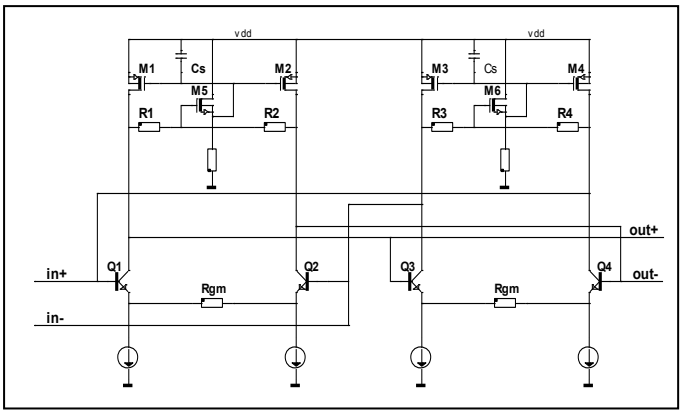

Fig.4 Gyrator implementation

V. TRUE TIME DELAY (TTD)

The antennas are placed on a grid (d=12mm), so the largest delay between two adjacent antennas is 57ps. This delay must remain constant over the entire IF-BW.

The TTD is based upon a traditional first-order all-pass filter body extended with an adjustable gain factor in the high-pass filter (HPF) branch to make it programmable, see Fig.5.

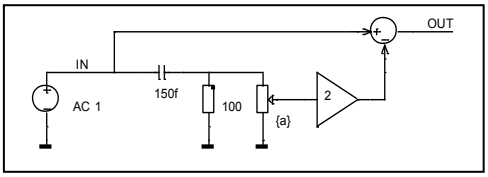

Fig.5. Prototype programmable TTD

Prototype simulations showed that in the IF-band (1-3GHz) the group-delay remains constant within 1ps over frequency for a delay between 0 and 33ps. Two of these cells cascaded can be used to reach the required 57ps. The TTD is also implemented with differential pairs and a Gilbert multiplier for wide-band performance, see Fig.6.

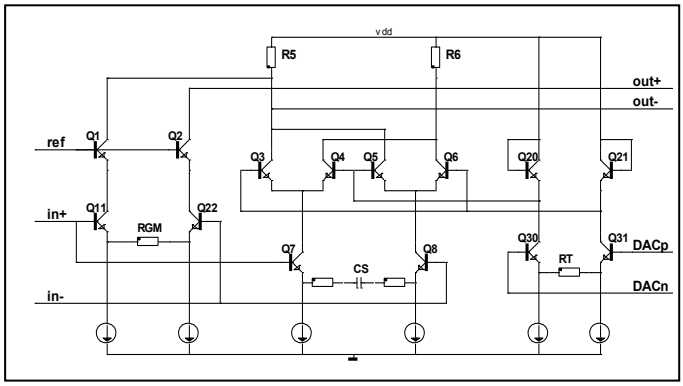

Fig.6 Implemented TTD

Q1/2 and Q11/22 present the direct path. Q7/8 present the HPF path, featuring a capacitor (CS) between the emitters. The output current of Q7/8 is fed into the multiplier and then subtracted from the currents of the direct path. R5/6 converts the sum-currents into the output voltage. The multiplier is controlled by the output currents of Q30/31. These transistors convert the controlling DAC voltage into a linear current via RT.

VI. POLARIZATION DISCRIMINATION

Fig. 1 shows how the satellites' H- and V-polarizations can be received by the antenna element. In our system we call the received signals X and Y to relate them to the board, not to the satellite. The antenna signals are two orthogonal components X/Y, each holding a part of the V and H (beam) signal.

Four channels receive the X-polarizations, the other four the Y-polarizations.

These X/Y signals are summed. Even though these signals are not representing H and V, they are still orthogonal and therefore can be rotated back to H/V by means of a vector modulator (Fig.7).

The modulator on chip uses four 4-quadrant Gilbert-cell VGA's according to:

$$V = -X.\sin(\alpha) + Y.\cos(\alpha) \quad H = X.\cos(\alpha) + Y.\sin(\alpha) \qquad (8)$$

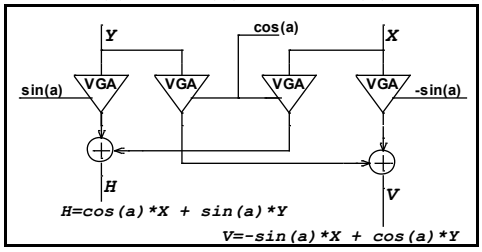

Fig.7 Vector modulator with VGA's

The measured discrimination exceeded 30dB.

VII. MEASUREMENT RESULTS

The overall channel transfer was measured with a R&S vector-network analyzer, the mirror suppression was measured at 17 dB while the simulation predicted 20dB, see Fig8:

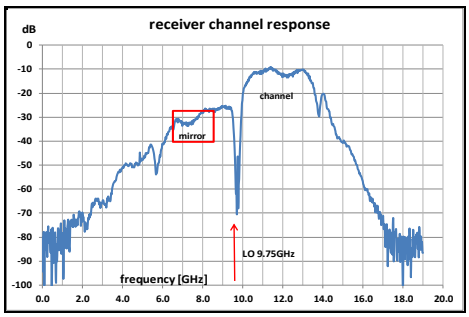

Fig.8 Measured overall channel response

The IF-filter response is compared to the simulation and has good agreement. The response of Fig.9 includes the test-board containing a balun at the IF-output:

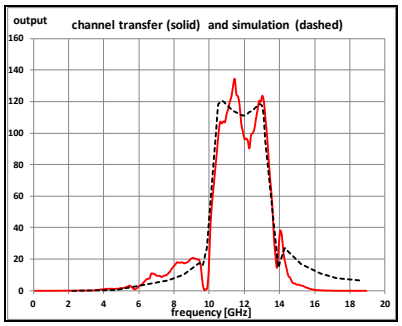

Fig.9 IF-transfer (linear scale) simulation (dash) and measurement (line)

The other 7 channels give comparable results. The data is summarized in Table-1. The compression point at the input (IP1dB) was found at -66dBm, see Fig.10:

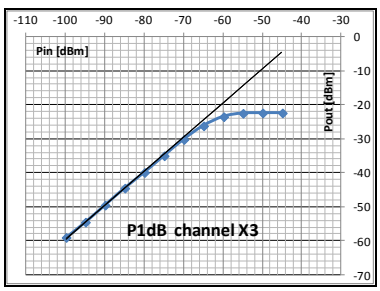

Fig.10 Measured 1dB compression point of channel X3

The OIP3 value is about -20dBm for all channels (Table 1).

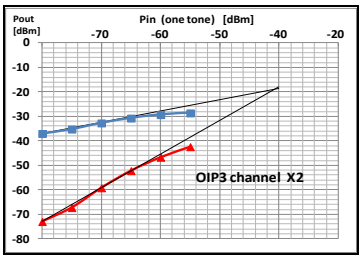

Fig.11 Measured OIP3 of channel X2

A channel to channel isolation test was done by driving channel Y3 (upper blue trace in Fig.12) and then switch off its last two stages (TT-delays) to prevent this signal to reach the adder. The channel Y4's output is measured, while the input is terminated with 50 ohms. The lower (red) trace is the combined feed-through of the channel-layouts and the off-state of two TT-cells. The difference is 40dB.

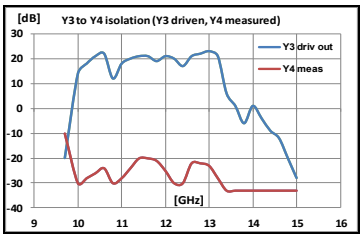

Fig.12 Measured channel to channel isolation

By switching off the LNA at the input of Y4 this value increased to 55dB. Evidently most of the cross-talk between channels is caused at the inputs. Another important parameter is the range of the programmable TT-delay cells. This was measured at 1 GHz IF-frequency , see Fig13:

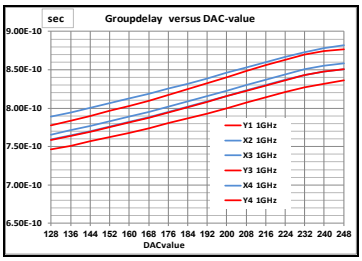

Fig.13 Measured max. TT-delay range versus DAC value

The linear range was ~80ps for 2 cascaded cells, more than simulated. The channel gain was predicted at 40dB, some channels have a bit less gain, as shown in Table 1.

Table 1. Measurements to date

CH #	IP1dB [dBm]	OIP3 [dBm]	Gain [dB]	Isolation [dB]	comment	NF [dB]	TT_off isolation
X1	-68	-19.5	40	-		11	60
Y1	-67	-20	39	38	X1 to Y1	11.2	65
X2	-64	-19	37	-		10.7	69
Y2	-62	-19	36	41	X2 to Y2	11	61
X3	-66	-19.5	41	-		11.1	71
Y3	-63	-20.5	35	-		-	73
X4	-66	-20	36	40	Y3 to Y4	-	69
Y4	-65	-20.2	37	-		-	75

The isolation of the last channel-cell when switched off (TT-delay cell) was measured and shown in the last column.

The chip photograph Fig.14 shows 2 square channel-layouts in each corner. At the mid of the left and right edges there are the LO drivers. At the top-mid the IF-output drivers are placed. Below those the adder is positioned. At the bottom-mid the SPI-bus is placed.

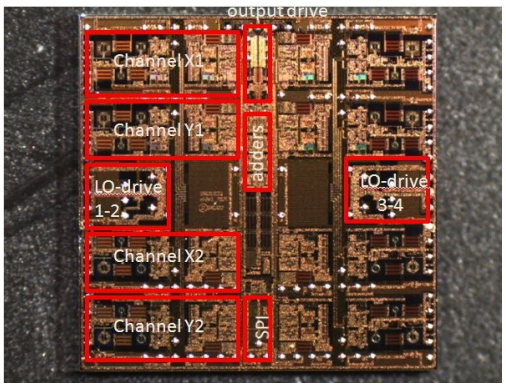

Fig.14 Chip photograph, die area is 3.8x4 mm

CONCLUSIONS

A 8-channel 12 GHz receiver chip can be created with all processing at IF-level, resulting in a power-consumption of only 132mW per channel. The radio channels have 40dB of gain and 17dB image rejection. OIP3 is better than -20dBm. A continuous programmable true time delay range of >66ps is realized. Differential-pair implementations with current-mode feedback are used and deliver a robust, high-speed and interference-free design on a 3.8*4mm die.

ACKNOWLEDGMENT

The author would like to thank J. W. Eikenbroek for his design efforts and NXP Nijmegen for the MPW run in QUBIC4Xi. The research described in this paper is funded by the Dutch Point One R&D Innovation Project: Broadband Satellite Communication Services on High-Speed vehicles.

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