TOWARDS AN OPTIMAL TRADE-OFF OF FUNCTIONAL REQUIREMENTS AGAINST SIZE, POWER AND COST FOR PHASED ARRAY ASICS

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***Abstract* – In this paper, we investigate various technologies and trade-offs used for manufacturing of integrated circuits with respect to their performance characteristics such as RF frequency, gain, noise figure, linearity and power consumption. This investigation is crucial for design of transceivers at microwave and higher frequencies. In the following, we show the in-house designed prototype of a highly integrated X- and K_u-band planar phased array receiver, having 8 channels and 64 antenna elements based on this investigation. The die size of the 8-channel phased array receiver with 2 GHz IF-bandwidth is 4 mm × 3.8 mm and the size of the prototype is 11 cm × 9.5 cm.**

I. INTRODUCTION

Today, the market for phased arrays is rapidly growing because of various applications such as high-speed broadband satellite internet services. This includes the emergence of in-flight connectivity (IFC), which is becoming a standard of many airlines [1]. To use different internet services on board, one crucial component is phased array antennas which are used to create beam-steering capability. On the other hand, a robust connection is achieved due to increasing the directivity of the antenna array. Moreover, phased arrays are preferred since they could provide a flat antenna solution without moving parts. Other applications include broadband internet for rural areas, marine and land mobile radio systems. A key challenge is to find optimum and affordable solutions when contemplating for mass production.

To obtain an optimised performance both for uplink and downlink, it is also necessary to invest on proper satellite systems which offer broadband services [2]. For example, Low Earth Orbit (LEO) and Medium Earth Orbit (MEO) satellites have better performance compared to geosynchronous equatorial orbit (GEO) satellites in terms of low latency and worldwide coverage.

As mentioned earlier, phased arrays are used to improve the performance of radio links. Although the 5G standardisation has not been finalised yet, it is obvious that phased arrays have an influential role for potential future 5G applications. For instance, beam-steering capability in base stations provides more reliable and broader bandwidth connections to all users located within the radio cells. The 5G time frame is not fully clear so far because its standardisation is still ongoing. A smooth transition to 5G is expected, with upgraded 4G (sometimes called 5G) already being offered now. Hence, it becomes crucial to provide ASIC solutions which meet advanced functional requirements, while also being affordable and having a low power consumption.

To provide a perspective, we present an overview of critical trade-offs which address to the most relevant parameters. Therefore, a wide range needs to be considered from process technology options for integrated circuit (IC) manufacturing to creation of phase lag/lead either by true time delay approach [3-4] or phase shift technique [5-6]. The performance of the most relevant parameters changes significantly from one process technology to another.

In this paper, we present a comparison between different trade-offs used for the design of a radio front-end in terms of critical parameters and process technologies when it is intended to design and fabricate ICs for X- (8-12 GHz) and K_u-band (12-18 GHz) applications. In Section IV, we present an example of a designed demonstrator for a mobile receiver of satellite TV based on different trade-offs discussed in Sections II and III.

II. Critical Trade-Offs for Parameters and Technology Nodes in IC Manufacturing

Different process technologies for IC manufacturing are selected based on their critical parameters such as cut-off frequency (f_t) and maximum frequency of oscillation (f_{max}), noise performance, substrate isolation, power consumption, breakdown voltage for transistors and integration capability. With respect to a specific application, also considering what critical parameters are more important than the others for that specific application, proper trade-offs is utilised accordingly. Hence, the trade-offs are not as straightforward as they may look like before taking the system requirements into consideration. For example, CMOS technology provides lower power consumption, high-speed switching due to high f_t/f_{max} (beyond 290/380 GHz, especially, for smaller nodes) and higher level of integration when contemplating to add digital circuitry into the same chip compared with SiGe BiCMOS and compound semiconductor technologies. However, CMOS technology suffers from higher substrate loss, and lower power handling and breakdown voltage for transistors compared with SiGe BiCMOS and compound semiconductor technologies.

When making trade-offs between different technologies, it is important to note that there is also a design choice in the amount of chip packages. Depending on the complexity of the application and the quantities needed, it may be better to use multiple chip packages rather than one. An example is the use of two separate chip packages with one for the RF front-end and another for the IF signal processing. Another trade-off is in the choice whether or not to integrate the LNA. However, there are some drawbacks by the use of multiple chip packages. For example, it is required to invest on different expensive electromagnetic (EM) tools. Furthermore, choose of newer technologies having smaller nodes is more expensive in terms of fabrication process.

It should also be noted that although CMOS technology is an expensive solution for chip fabrication, the number of samples are obtained from a silicon wafer is more than the other process technologies. Thus, CMOS process is suitable for mass production.

III. Example of a Design Trade-Off: Choice Between True Time Delay and Phase Shift

One of the critical trade-offs in a phased array system is phase shift implementation by the use of active and passive components. Active phase shifters provide continuous and digital phase shift in a more compact design compared with passive phase shifters, especially, at lower frequencies. Active phase shifters, however, meet some challenges such as design complexity, high power consumption and extra parasitics due to the use of active components which becomes more critical at higher frequencies. Passive phase shifters achieve better linearity and higher power handling compared with active phase shifters. However, the size of passives compared to the wavelength becomes more challenging at lower frequencies.

Moreover, in a radio front-end, another trade-off needs to be considered by placing phase shifters either in the LO path [7-9], or IF path [10-11] or RF path [12-14]. For instance in a receiver front-end, for RF and LO phase shifting schemes (Fig. 1), each IF path requires a separate frequency converter. Thus, the LO and RF distribution networks get complicated for larger number of IF paths.

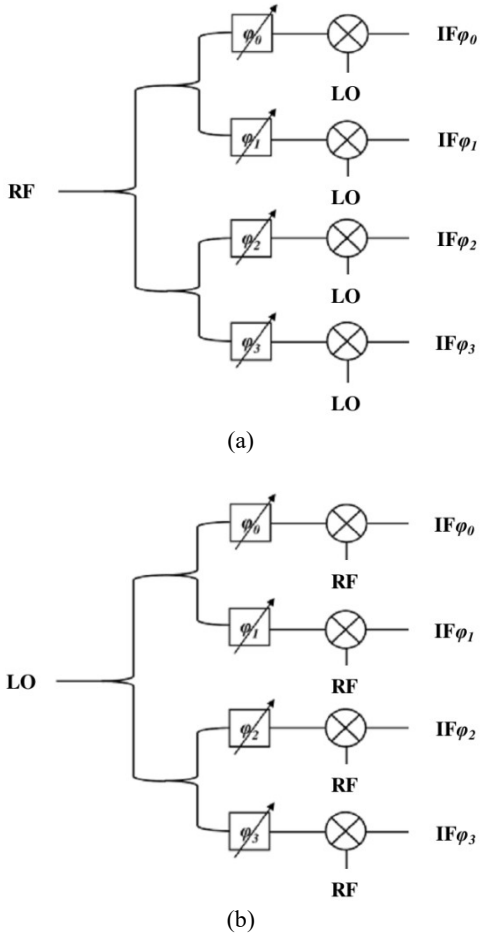

Figure 1. Block diagram of phase shifting implementation using RF path (a) and LO path (b) schemes

For the IF phase shifting scheme, the frequency converter is shared among the IF paths which results in a simple system architecture, especially when an extension to large array implementation is desired. In addition, the final design occupies a smaller chip area compared to the RF and LO phase shifting schemes due to the use of less circuit blocks. Fig. 2 represents the block diagram of an IF path phase shifting scheme.

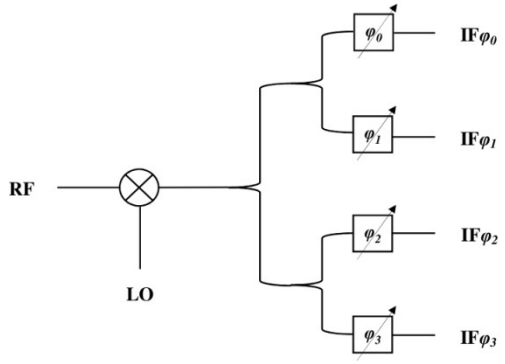

Figure 2. Block diagram of phase shifting implementation in IF path

Next critical trade-off is how the phase shift creation is utilised in the desired path (RF, LO, or IF), which was mentioned earlier. Typical techniques are true time delay and phase shift [3-6]. True time delay is more preferable rather than phase shift implementation. First, the phase shift implementation makes it frequency dependent. Hence, the beam direction varies within the received bandwidth. This phenomenon is called beam squint. Second, for a very directive and narrow beam, squint cannot be tolerated when the bandwidth is wide. Therefore, a true time delay is preferred since it has a constant delay over the entire bandwidth.

As a system trade-off, it is required to choose an appropriate type for the antenna. As mentioned earlier, in-flight communication services require high data-rate links which demand higher frequency bands [15]. For instance, at X- and K_u-band, 10.7 to 12.75 and 14 to 14.5 GHz with dual-polarised capability can be used for receive and transmit purposes, respectively [16]. To implement the IFC services on an aircraft, the antenna is required to have a full hemispherical coverage for the main beam. Furthermore, a 90°-scan surpassing from zenith is necessary to account for pitch and roll of the aircraft [17]. Although there are several antenna architectures which satisfy these requirements, they have several impacts on the aircraft fuselage such as aerodynamic considerations and increasing the electrical and mechanical complexity. Hence, a flat antenna array solution as shown in Fig. 3 is proposed to satisfy the system requirements.

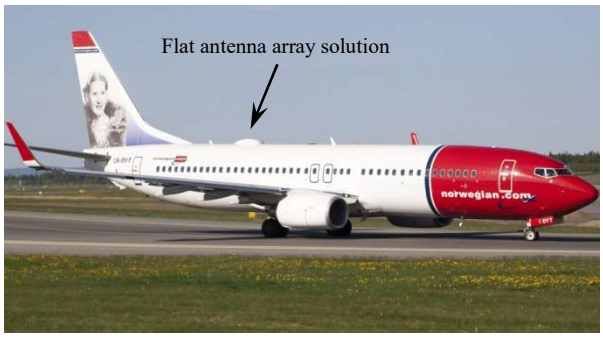

Figure 3. In-flight connectivity with flat antenna array solution in a moving vehicle

Another system trade-off is the design of a radio front-end either by zero-IF or low-IF methods. For example, zero-IF is suitable where the RF/IF bandwidth is narrow [18]. It provides easier implementation, for instance, in the design of the IF low pass filter. Zero-IF, however, imposes few drawbacks on the system such as increasing the power consumption and the complexity of the design. For example, it requires signal processing over a broader frequency range of implementation. Some benefits and drawbacks of each method are shown in Tab. 1.

Table 1. Advantages and disadvantages of zero and low IF techniques

Zero-IF	Low-IF
Pros: – Simpler IF low pass filter **Cons:** – Strong LO leakage into high gain IF – Signal processing over log(2GHz/1Hz) = 9.3 decades frequency range – Only image rejection from I/Q mixer – DC offset	**Pros:** – LO frequency outside IF filter – Signal processing over log(2GHz/1GHz) = 0.3 decades frequency range – Image rejection extended with LNA selectivity **Cons:** – Complex IF band pass filter

As reported in [19-20], a highly integrated X- and K_u-band planar phased array receiver, having 8 channels and 64 antenna elements has been designed in-house and fabricated with respect to the trade-off aspects which have been discussed so far. Since the IF bandwidth is as wide as 2 GHz and beam squint is forbidden, true time delay has been utilised compared to phase shift. This demonstrator is a good example that shows different trade-offs between critical

parameters during the design and manufacturing phases.

IV. Results from Prototype True Time Delay Receiver

The fabricated demonstrator as reported in [19-20], is shown in Fig. 4. It is a successful design of a phased array receiver front-end at X- and K_u-band with full functional chips fabricated by SiGe BiCMOS and GaAs technologies. The phase creation is carried out by implementing true time delay which allows the receiver tile to combine 4×4 antenna elements in the IF domain (2 GHz bandwidth). Moreover, true time delay prevents beam squint and allows a broader bandwidth, resulting in instantaneous reception over the entire band for dual-polarisation with full scan angle. Tab. 2 represents the performance summary of the demonstrator.

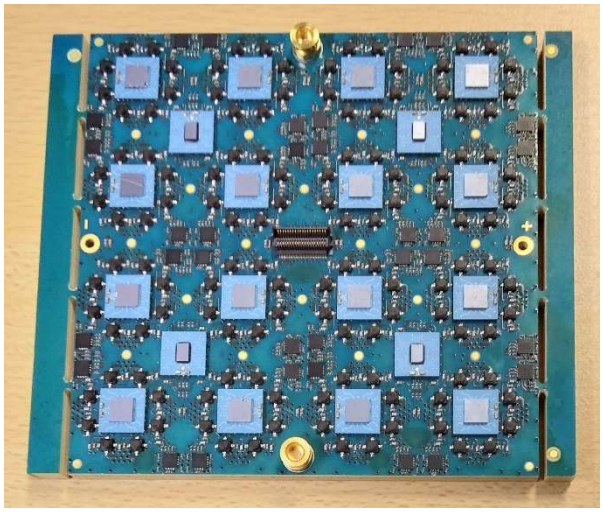

Figure 4. Prototype of the fabricated receiver and antenna tile. The total size is 11 cm × 9.5 cm

Table 2. Performance summary of the designed phased array receiver [20]

Operating frequency [GHz]	10.7–12.75
Gain/channel [dB]	40
IF bandwidth [GHz]	2
IP_{1db} [dBm]	-66
Delay range [ps]	0–100
Power consumption [mW]	132
Die size for 8-channel phased array receiver [mm^2]	15.2
Demonstrator size [cm^2]	104.5

V. Conclusion

Different trade-offs with respect to their critical parameters have been reported in this paper. A wide range of trade-offs from size and cost to system performance needs to be fully taken into consideration for applications which are coming up in the market. For example, cost breakthrough for large volume production can be achieved by using CMOS technology which has a comparable performance, especially for smaller nodes on critical parameters, compared to compound semiconductor and SiGe BiCMOS technologies.

The 8-channel phased array receiver, shown in this paper, has been designed by utilising true time delay approach which provides wider bandwidth and prevents squinting of the beam compared with phase shift approach. Thus, the instantaneous reception over the entire band is achievable for dual-polarisation with full scan angle. The ASICs and external LNAs on the prototype have been fabricated by SiGe BiCMOS and GaAs technologies, respectively due to the trade-off for the noise performance. The design shows promising results, therefore, the discussed critical trade-offs could be implemented to realise the whole transceiver front-end.

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