Design of a highly integrated Ku-band planar broadband phased array receiver with dual polarization

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Abstract—A highly integrated Ku-band (10.7 – 12.75 GHz) planar phased array receiver of 64 antenna elements is presented. It features instantaneous reception of the full Ku-band (2.05 GHz wide) in two orthogonal polarizations with scan angles up to 75 degrees by using time delay instead of phase shift. The receiver is part of a system for satellite reception on board of moving vehicles. Two SiGe RFICs were developed, packaged in ceramic BGAs and assembled onto a 15-layer PCB which integrates the antenna elements. An outline of the system is given along with a detailed description. It sets a new standard in integration density.

Keywords—Phased arrays; Receiving antennas; Satellite communication; Wideband

I. INTRODUCTION

Broadband wireless communication has become common in our everyday life. While in-flight entertainment has been available, live video and internet are introduced in aircraft only recently.

The currently available systems are mechanically or hybrid mechanically / electronically steered antennas which operate in the Ku-band. In [1] a path towards structural integration of antennas is presented, based on a fully electronically steered array. Different system architectures have been studied in [2], where a system consisting of 24 antenna tiles with 8x8 antenna elements (AEs) is proposed. Achieving the required level of integration remains a big challenge with the previous limit being reached by [3] with LNA, phaseshift, summation, filtering, downconversion and antenna for an 8x8 array with one linear polarization on a single 98x98mm PCB and by [4] with LNA, phaseshift, frequency discrimination and antenna for 156 dual polarized AEs on a single 20cm diameter PCB.

This paper presents another major step in functionality and integration with 128 Ku-band inputs on a 94x94mm footprint (i.e. 1.45 channels/cm²). It features both polarizations along with a polarization discriminator which is required for a mobile terminal. To the best of our knowledge this is the first time such a highly integrated planar Ku-band receiver tile is presented and demonstrated.

This major improvement is realized with two SiGe RFICs which have been designed and manufactured in this project along with bespoke LTCC CBGA packages. A novel implementation of electronical true time delay (TTD) is used in these RFICs, allowing the receiver tile to combine 4x4 AEs in the IF domain. A new RF-board stackup consisting of 15 metal layers is devised, designed and manufactured which integrates both antenna and RF electronics. Further beamforming is performed by an optical beam forming network (OBFN).

Architecturally the system has been designed such that it can easily be modified to support dual-beam operation (Fig. 1), each beam being restricted to a single (but not fixed) polarization. This allows a single antenna to provide seamless handover between different satellites.

II. SYSTEM OVERVIEW

The architecture (Fig. 2) consists of 24 receiver tiles, an OBFN, LO generator (9.75 GHz) and a controller / power supply. It features 4x4 sub-arrays with downconversion and local IF beamforming (TTD) before optical beamforming (OBFN). The use of time delay prevents squinting of the beam, resulting in instantaneous reception of both polarizations over the full bandwidth and scan angle.

Fig. 1. Multibeam operation of a phased array.
A receiver tile (Fig. 3) consists of an array of 8x8 dual polarization AEs with GaAs LNAs which are combined by the two distinct RFICs in bespoke packages. This is all (including signal distribution and glue components) integrated on / in a single PCB measuring 94x94mm with a thickness of 10mm.

The AE concept is discussed in [5] and updated for the PCB stackup used in this project. To achieve the required bandwidth an AE uses two stacked patch resonators excited by two offset feedlines coupled through a dog-bone aperture. It receives both X and Y polarization (related to the antenna, not to the satellite).

A discrete Ku-band GaAs LNA follows because the noise figure (NF) requirement of <2 dB cannot be met by the RFICs alone. It is biased from a single positive supply by a commercial bias controller. In literature a single NF is normally given which indicates the NF for a broadside beam (0.6dB in our case.) In practice the NF will change along with the AE impedance over scan angle, the worst case NF due to scan should be used in system performance calculations, which is 0.9dB in this system. The gain requirement of the tile is 60dB of which 10dB is realized by this LNA.

RFIC1 combines 4 AEs (4X and 4Y input signals). Each single ended input has its own channel providing low noise amplification, down conversion, IF filtering, phase shift and time delay. After summation there is polarization discrimination and a variable gain amplifier. This results in a H and a V output, both differential IF signals between 0.95 GHz and 3 GHz. It has 35dB conversion gain. RFIC1 is described in detail in [6]. 16 of these RFIC1s are used.

Groups of 4 RFIC1s are combined by RFIC2 (4 in total) which provides an input buffer, additional time delay, summation and a variable gain output buffer. Gain for this device is 15dB at IF.

The above gives a total of 4 differential outputs for each polarization which are transferred from the tile to the OBFN through a single 40 pin 0.5mm pitch connector which also serves the digital communication bus. The OBFN combines a number of tiles into two output signals ready for a modem or broadcast receiver. Ref. [7] outlines the principle and design of the OBFN. It uses a single laser, modulators, optical ring resonators (ORRs) and a balanced detector.

Thermal performance has not been simulated in this stage of the project. The OBFN is thermally driven and therefore needs a stable base temperature. As this OBFN is connected directly to the receiver tile, the exposed RFIC-die backsides can have thermal contact with the OBFN baseplate through an interface layer. The smaller parts like GaAs LNA and bias controllers have low dissipation and can cool by radiation.

III. BOARD DESIGN

The following is integrated in or assembled onto the RF PCB:
- 64 AEs with two polarizations each
- 128 discrete GaAs LNAs with biasT’s
- 32 bias controllers for the GaAs LNAs
- 16 RFIC1s
- 4 RFIC2s
- LO distribution
- RF rerouting
- IF routing
- DC and control routing
- LO, IF, digital and DC connectors

The vast amount of RF, IF and LO signals to be routed along with the requirements on isolation (30dB) resulted in the 15-layer stack up of Fig. 4. Despite the high number of layers and use of high frequency laminates it is designed to only use mainstream PCB process steps and tolerances to keep the cost down. 64 AEs are integrated in the antenna part of the PCB. This is a vast cost saving, but constrains component placement to a single side.

The RF stripline follows where bias-Ts are placed for the gates of the GaAs LNAs and where the antenna signals are rerouted to the positions needed at the component side. All signals are kept equal in length and reflection characteristics. If these paths differ there will be an amplitude and phase ripple which is different from AE to AE, giving a variation in beam shape (including pointing error) over frequency.
A second stripline follows for LO distribution and IF routing (between RFICs and the output connector.) Each RFIC1 has two LO inputs (32 in total.) These are distributed from two coaxial LO input connectors by means of unisolated splitters. This keeps the PCB simple, but VSWR interaction gives power and phase differences. RFIC1 is insensitive to these power variations and can correct the phase variations.

A layer is used for routing a reference voltage and a digital serial bus to the RFICs and gate and drain bias voltages for the GaAs LNAs. Below this the supply plane is realized powering all components from a single common positive supply. The bottom serves as microstrip for routing the RF signals and drain bias-Ts as well as being the component side.

Many high frequency board transitions were designed and simulated with a 3D EM solver to have a reflection of < -20 dB. The vertical transitions mainly use a coaxial mode. A part of the via bus is removed by drilling it away after plating (Fig. 4 and Fig. 5). This back-drill process reduces the number of required drilling and plating steps, making the board more manufacturable, accurate and affordable. A drawback is that part of the via remains after back-drilling (a stub) which varies in length due to tolerance on board thickness and drill depth. Inductive compensation (Fig. 5) is designed for a stub length of 0.15mm, giving good performance up to 0.3mm length.

Each part of the stack has been given its own shielding vias to provide sufficient isolation while preventing these vias from interfering with routing in other layers. Where possible vias through multiple parts are used to make sure the intermediate dielectric layers (e.g. the one between both striplines) do not provide a propagating path or resonance.

At first SMP connectors were considered for the IF outputs (16 in total.) Due to the high cost and the board area they would occupy (576 mm²) an alternative was found in a connector from FCI (Fig. 6.) This is cheap and small (72mm² for all IF outputs and the digital communication.) Measured performance is given in Fig. 7. The blue trace represent two Baluns in series, the red trace includes the connector. Isolation is given by the green (adjacent) and purple (opposite) traces (note; both on the right axes.)

IV. CBGA PACKAGE DESIGN

Two packages were designed, one for each RFIC. The package has been constructed of two main layers of LTCC. The bottom is covered by overglaze while a thin LTCC layer is used at the top to act as soldermask and to confine the EM field close to the microstrip transmission lines, aiding isolation. Routing on the package features equal length for all RF and IF signals.

The chip has been balled and flip chip mounted to the package (Fig. 8) with underfill for environmental and mechanical protection. Both packages are 9x9 CBGAs with 1mm pitch and 0.7mm non collapsible balls.
Even though it is perfectly possible to use bond wires for signal transfer, the flip chip gives better isolation (no radiating bond wires) and lower inductance from the supply planes to different chip blocks. Both the positive supply and the ground are available underneath the chip which makes it possible to keep them separated on-chip to prevent coupling. All transitions to the PCB and to the RFICs have been simulated with a 3D EM simulator and designed to give < -20dB reflection and > 30dB isolation.

V. COMPARISON

The significance of the work in this paper is in the level of integration. Ref. [3] and [4] are similar in intended function and therefore the main functional parameters are comparable (Table 1.) This work sets a new standard in number of channels per area (Density (ch/cm2)) and DC power consumption per channel (Pdc (mW/ch)). It is worth noting that this DC power includes a high level of gain and functionality (including down conversion, polarization discrimination, phase correction and first level beamforming.)

The noise figure (NF) as listed in this work is simulated over the full antenna scan angle to give realistic performance expectations. Unfortunately these numbers were not available in the references.

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<th>TABLE I. COMPARISON</th>
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<td>Frequency (GHz)</td>
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<tr>
<td>10.7 - 12.75</td>
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<tr>
<td>Polarization</td>
</tr>
<tr>
<td>Channels (ch)</td>
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<tr>
<td>Area (cm2)</td>
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<td>Density (ch/cm2)</td>
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<td>Pdc (mW/ch)</td>
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<td>Gain (dB)</td>
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<td>NF (dB)</td>
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* Over full scan angle and including antenna loss

VI. FUTURE WORK

At the time of writing all components including the PCB have been manufactured. In the short term the demonstrator tile will be assembled and measured as well as RFIC2 and further characterisation of RFIC1 will be performed.

With the required level of integration and functionality being achieved, the next iteration should focus on further cost reduction. While the current PCB stackup uses common materials and processing and manufacturability is proven, the sheer number of layers prevent it from becoming truly low cost. Reducing board complexity is possible by integrating the GaAs LNA bias controller onto RFIC1. In [8] a full PLL is presented in the same IC process. It is small enough to integrate onto RFIC1, removing the need for LO routing in the board.

Finally a minor change in RFIC1 and its environment will support multi-beam operation.

VII. CONCLUSION

A highly integrated receiver tile has been presented covering the full Ku-band instantaneously in both linear polarizations. It sets a record in integration density, made possible by two SiGe RFICs in CBGA packages on a multilayer PCB integrating the antenna. The design along with the chosen architecture and technology pave the way towards an affordable structurally integrated multi-beam phased array antenna on moving vehicles.

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REFERENCES